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(54) **OPTICAL RECEIVER**

OPTISCHER EMPFAENGER

RECEPTEUR OPTIQUE

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(56) References cited:
**US-A- 4 757 192**

- **Patent Abstracts of Japan, Vol 11, No 329, E-552, 1989-11-07, abstract of JP, 62-115902 (NEC CORP.),**
- **Patent Abstracts of Japan, Vol 13, No 531, E-851, 1989-11-07, abstract of JP, 01-216606 (YOKOGAWA ELECTRIC CORP.),**



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## Description

### Field of the Invention

The present invention relates to an opto-electronic receiver apparatus for use in an optical fiber communications network. More particularly, the present invention relates to methods and apparatus for achieving an optical receiver with increased dynamic range.

### Background of the Invention

Transimpedance amplifiers are employed in optical receivers in order to convert very small currents indicative of optical signals applied to photodiode detectors. These small currents are then converted to signal voltages of greater amplitude. In an optical fiber communications network whereby a plurality of geographically distributed users each write onto a common optical fiber, incoming optical signals from a nearby transmitter may be detected at a high signal level, whereas incoming optical signals received from a distant transmitter may be detected at very low signal levels. Thus, to be effective, a transimpedance front end of the optical receiver must be sufficiently sensitive effectively to receive the weakest optical signals and must also be controllable to receive the strongest optical signals without reaching saturation and resultant distortion in the detected signal voltages.

High sensitivity and high saturation level are contradictory requirements for a transimpedance front end of an optical receiver. A simplified representation of a typical transimpedance front end of an optical receiver is illustrated in Fig. 1. With reference to the Fig. 1 configuration, if the amplification factor -A is sufficiently large, the transimpedance is equivalent to the feedback resistance $R_L$. On one hand, for high sensitivity the $R_L$ value should be large because the noise current introduced by the feedback resistor is inversely proportional to the resistor value. On the other hand, to realize a high saturation level, the value of $R_L$ should be small in order to limit signal excursion.

Techniques reported in the prior art for increasing dynamic range improvement typically involve the use of active devices at sensitive nodes of the transimpedance amplifier. One example is given in Fig. 2. In Fig. 2, an FET device is provided at the input of the amplifier to shunt away photo current at high signal levels to prevent saturation of the amplifier. In Fig. 3, an FET device is shunted across a portion $R_{L1}$ of the feedback resistor $R_L$ in order to lower the value thereof at high signal levels. The FET devices employed in these prior art examples are placed at sensitive nodes, i.e. the input of the amplifier in Fig. 2 and across the feedback resistor in Fig. 3. The FET devices add parasitic capacitances into the amplifier circuit, and these parasitics have a significant effect upon the performance of the overall amplifier circuit. In order to minimize the effect of the parasitics, the characteristics of the FET devices must be chosen carefully and tightly controlled within a narrow tolerance. Usually, the FET devices have been incorporated into an integrated circuit amplifier wherein the design of the active device may be customized for a particular application.

Neither of the techniques illustrated in Figs. 2 or 3 for extending the dynamic range of an optical receiver is convenient if the designer is limited to standard "off the shelf' discrete circuit components and elements.

US Patent 4,757,192 discloses an extended dynamic range optical receiver and signal amplifier apparatus comprising a photodetector, a buffer connected to the photodetector and an amplifier connected to the buffer for amplifying the signal of the photodetector. The amplifier comprises two feedback networks, wherein one of these networks comprises a switch connected to the input of the amplifier and used to connect this network in parallel with the other feedback network. The apparatus further comprises an optical level sensing and switching control means connected to the photodetector, by means of which the switch provided in the one feedback network is controlled.

### Summary of the Invention

The object of the invention is to provide a transimpedance front end for an optical receiver with increased dynamic range without the problems of a switch coupled to the input of the amplifier. Thereby the invention allows to realize the transimpedance front end with standart "off-the-shelf" electronic components, with a minimum of circuit complexity and at relatively very low cost.

In accordance with the present invention a transimpedance front end is provided for an optical receiver including a photodetector coupled optically to an optical fiber for receiving optical signals over the fiber and connected electrically to the front end, wherein the front end comprises:

a buffer connected with its input to the photodetector,
a first amplifier connected with its input to the output of the buffer through first switching means and comprising a first high value feedback resistor means connected between the output of the first amplifier and the input of the buffer to define a first mode low optical signal level amplifier configuration,
a second separate amplifier connected with its input to the output of the buffer through second switching means and comprising a second low value feedback resistor connected with its one side through a third switching means to the output of the second separate amplifier and with its other side to the input of the buffer to define a second mode high optical signal level amplifier configuration, and
optical level sensing and switching control means connected to the photodetector for sensing an in-

coming optical signal level and to the first, second and third switching means for switching between the first and second amplifier configurations as a function thereof.

According to another aspect of the invention, a transimpedance front end is provided whereby a switch is incorporated into the amplifier to selectively switch between an open and closed circuit configuration dependent on a sensed current level to be amplified, with first and second separate and independent amplifiers being provided and first and second separate and independent feedback resistors being provided so that one amplifier is capable of operating during one mode (low gain) and the other amplifier is capable of operating during another mode (high gain). The low gain amplifier and feedback resistor comprise passive and active components which are all separate from those forming the high gain amplifier and feedback resistor (except for interconnect conductors).

These and other objects, advantages, aspects and features of the present invention will be more fully understood and appreciated upon consideration of the following detailed description of preferred embodiments, presented in conjunction with the accompanying drawings.

## Brief Description of the Drawings

Fig. 1 is a simplified block and schematic circuit diagram of a conventional transimpedance front end of an optical receiver.

Fig. 2 is a simplified block and schematic circuit diagram showing one approach of the prior art for extending the dynamic range of the Fig. 1 front end.

Fig. 3 is a simplified block and schematic circuit diagram showing another approach of the prior art for extending the dynamic range of the Fig. 1 front end.

Fig. 4 is a simplified block and schematic circuit diagram illustrating a transimpedance front end of an optical receiver incorporating principles of the present invention.

Fig. 5 is a more detailed schematic circuit diagram of the Fig. 4 transimpedance front end.

## Detailed Description of the Preferred Embodiment

Fig. 4 illustrates in overview an improved transimpedance front end 10 of an optical receiver which achieves extended dynamic range while employing standard, low cost transistors and other components in a noncritical manner. A photodiode 12 is connected to the input of a buffer amplifier 14. In a first operational mode adapted to high gain amplification of low signal levels, the buffer amplifier 14 connects to an amplifier 16 through a switch 18. The amplifiers 14 and 16 form a transimpedance amplifier by virtue of a feedback resistor 20 which has a relatively large value.

When the detected optical signal reaches a value where maximum sensitivity is no longer required, the first operational mode including amplifiers 14 and 16 is discontinued, and a second operational mode suitable for handling large magnitude optical signals without saturation is established. In the second mode, a transimpedance amplifier is obtained by the configuration of the buffer 14 and an amplifier 24 connected to the buffer 14 via a switch 22. A small value feedback resistor 26 is also connected via a switch 28 from the output of the amplifier 24 to the input of the buffer 14. By substituting the second mode configuration with the low value feedback resistor 26, the saturation level of the transimpedance front end 10 is extended. Since the optical signal is now large, the low value of the resistor 26 does not adversely affect overall performance of the optical receiver. Signal voltage output is provided via an analog demultiplexer circuit 30.

An optical level detector includes a sense resistor 32 and a capacitor 34 which are connected to receive the photo current input from the photodiode 12. The sense resistor develops a voltage which is proportional to the average photo current and this voltage is compared with a reference voltage $V_R$ by a comparator circuit 36. The comparator 36 provides a control output 38 which operates the switches 18, 22 and 28 to switch the front end 10 from the first mode to the second mode when the incoming optical signal level exceeds the reference voltage $V_R$ which is a known, preset value, and similarly the comparator operates the switches to switch the front end 10 from the second mode to the first mode when the overage value of the incoming signal falls below the reference voltage $V_r$.

The capacitor 34 along with resistor 32 provide a sufficiently long time constant so that the sense voltage represents the average optical signal power. Also, hysteresis is provided in the switch control function so that the control does not dither between the two operational modes.

Fig. 5 provides a practical implementation of the Fig. 4 circuit 10. The same reference numerals employed above to describe Fig. 4 are also employed to identify corresponding functional areas and elements of the Fig. 5 circuit implementation. In the Fig. 5 example, three switch transistors Q2, Q3, and Q6 switches between essentially an open circuit and closed circuit state depending on the sensed current level to be amplified. Transistor Q2 switches amplifier 16 and high gain resistor 20, Q3 switches amplifier 24, and Q6 switches low gain resistor 26.

Transistor Q8 and Q9, 39 form a "current mirror" which reflects the photocurrent representing the average optical signal power into the comparator circuit 36.

The buffer amplifier 14 is implemented as a GaAs MESFET transistor Q1. In the first operational configuration for low optical signal levels, the buffer Q1 is coupled to amplifier 16 formed by NPN transistor Q5 and PNP transistor Q2 through the switch 18 including PNP

transistor Q2 and comparator 18 (U1B). Transistor Q2 acts in a dual role as part of amplifier 16 and switch 18.

For low level signals below a reference voltage level set by the comparator 36 (implemented as a first one U1A of a four open-collector comparator array, such as type LM 2901), the output control signal on line 38 is low. This causes the output of the comparator U1B to be low and the switch transistor Q2 to be conducting, resulting in coupling of the output from the buffer Q1 to the base of transistor Q5.

At the same time, the low gain configuration formed by circuit elements 22, 24, 26 and 28 is inactive. Switch 22 includes a third comparator U1D which controls the base of an PNP switch transistor Q3. In the high gain configuration, the output of the third comparator U1D is high, causing the transistor Q3 to be in a high impedance state thereby causing Q4 to cut off and causing diode CR1 to be reversed biased. Similarly, the switch 28 disconnects the low value resistor 26 (12K ohm) from ground (Grd). The switch 28 includes a fourth comparator U1C, a switching transistor Q6 and diode CR1. In this mode the output of the fourth comparator U1C is low which removes the base bias from the transistor Q6, and Q6 also presents a high impedance. The net effect is to eliminate any conduction path for current through the low value resistor 26. Thus, the first operational mode results in a sensitive, high gain transimpedance amplifier comprising the Fig. 5 elements Q1, Q2, Q5, Q7 and feedback resistor 20 configured as a 150K and 10K resistor in series. The output buffer 30 comprising the element Q7 and wire "O-ring" of Q5 and Q4 operating in this first circuit configuration.

When the optical signal reaches a significant level, such as -26 dBm, the level detector 36 (U1A) changes from low to high. U1B now goes high, turning off Q2 and opening the path between the buffer transistor Q1 and the amplifier 16 (Q2, Q5). This disables the high gain configuration. Concurrently, the switch 22 turns on, thereby connecting the buffer Q1 to amplifier 24 (comprising an PNP transistor Q3 and the NPN transistor Q4). Also switch 28 turns on (U1D goes high, forward biasing transistor Q6, which also causes the emitter-base junction of transistor Q5 to become forward biased, resulting in connection of the low value resistor 26 in the circuit. The low gain amplifier configuration (resistor 26, Q3, Q4) is now activated, thereby increasing the saturation level of the optical receiver. As with the high gain amplifier configuration, transistor Q2 acts as a dual role as part of amplifier 24 and switch 22.

With the dual mode optical receiver thus realized, a sensitivity of -43dBm, a saturation level of -10dBm, and an overall dynamic range of 33 dB is realized. The Fig. 5 circuit implementation is realized with standard off-the-shelf components. The NPN transistors Q4, Q6, and Q7 may be type MPSH 10 or equivalent. The PNP transistors Q2, Q3, may be type MPSH 81 or equivalent. The quad comparator implementing U1A, U1B, U1C and U1D may be type LM2901, or equivalent. The other circuit elements have the values associated proximately with their symbols as shown in Fig. 5.

## Claims

1. A transimpedance front end (10) for an optical receiver including a photodetector (12) coupled optically to an optical fiber for receiving optical signals over the fiber and connected electrically to the front end (10), the front end (10) comprising:

   a buffer (14) connected with its input to the photodetector,
   a first amplifier (16) connected with its input to the output of the buffer (14) through first switching means (18) and comprising a first high value feedback resistor means (20) connected between the output of the first amplifier (16) and the input of the buffer (14) to define a first mode low optical signal level amplifier configuration,
   a second separate amplifier (24) connected with its input to the output of the buffer (14) through second switching means (22) and comprising a second low value feedback resistor (26) connected with its one side through a third switching means (28) to the output of the second separate amplifier (24) and with its other side to the input of the buffer (14) to define a second mode high optical signal level amplifier configuration, and
   optical level sensing and switching control means (32, 34, 36) connected to the photodetector for sensing an incoming optical signal level and to the first, second and third switching means for switching between the first and second amplifier configurations as a function thereof.

2. The transimpedance front end (10) as claimed in claim 1, wherein each amplifier (16; 24) comprises at least two amplification transistors (Q2, Q5; Q3, Q4).

3. The transimpedance front end (10) as claimed in claim 1 or 2, wherein the first amplifier (16) comprises a first transistor (Q2) operating in a dual mode as the first switching means (18) to selectively connect the first amplifier (16) to the buffer (14) and as an amplification transistor to amplify a signal when the first amplifier configuration is selected by the optical level sensing and switching control means (32, 34, 36), the second amplifier (24) comprises a second transistor (Q3) operating in dual mode as the second switching means (22) to selectively connect the second amplifier (24) to the buffer (14) and as an amplification transistor to amplify a signal when the second amplicication configuration is selected

by the optical level sensing and switching control means (32, 34, 36).

4. The transimpedance front end (10) as claimed in claim 3, wherein each amplifier (16; 24) includes a separate additional amplification transistor (Q5; Q4).

5. The transimpedance front end (10) as claimed in claim 3 or 4, wherein each amplifier (16; 24) includes a comperator (U1B; U1D) having an output coupled to its respective dual mode transistor (Q2; Q3), an input of the comparator (U1B; U1D) being connected to the optical level sensing and switching control means (32, 34, 36).

6. The transimpedance front end (10) as claimed in any one of claims 1 to 5, wherein the third switching means (28) includes a switching transistor (Q6) for selectively switching the connection between the low value feedback resistor (26) and the second amplifier (24) between essentially an open circuit and closed circuit configuration.

7. The transimpedance front end (10) as claimed in any one of claims 1 to 6, wherein the optical level sensing and switching control means (32, 34, 36) includes means for averaging a value of a sensed optical signal level and includes time constant means producing a time constant being sufficiently long to prevent dither switching between the first and second level amplifier configurations.

8. The transimpedance front end (10) as claimed in claim 1, wherein the high value feedback resistor means (20) defines a resistive feedback path which does not include any part of a resistive feedback path defined by the low value feedback resistor means (26).

9. The transimpedance front end as claimed in claim 1, further comprising an input node, wherein

the photodetector (12) is connected to the input node,
the buffer (14) comprises a buffer transistor (Q1) having a base electrode connected to the input node and having a collector output,
the first switching means (18) includes a first switch transistor (Q2) having an emitter-collector signal path connected to said collector output, and a first comparator (U1B) for controlling a base electorde of said first switch transistor (Q2) in accordance with a switching control signal (38) produced by the optical level sensing and switching control means (32, 34, 36),
the first amplifier (16) comprises a first transistor amplifier means (Q5) having an input connected to the emitter-collector signal path of the first switch transistor (Q2) and having an output connected to an output buffer (Q7),
the first high value feedback resistor means (20; R2, R3) is connected from the output of the first transistor amplifier means (Q5) to the input node,
the second switching means (22) includes a second switch transistor (Q3) having an emitter-collector signal path connected to said collector output, and a second comparator (U1D) for controlling a base electrode of said second switch transistor (Q3) in accordance with the switching control signal (38),
the second amplifier (24) comprises a second transistor amplifier means (Q4) having an input connected to the emitter-collector signal path of the second switch transistor (Q3) and having an output connected to the output buffer (Q7), and
the second low value feedback resistor means (26) is connected from the output of the second transistor amplifier means (Q4) through said third switching means (28) to the input node,
wherein said third switching means (28) includes a third switch transistor (Q6) and a third comparator (U1C) for controlling a base electrode of the third switch transistor (Q6) in accordance with the switching control signal (38).

**Patentansprüche**

1. Transimpedanz-Eingangsstufe (10) für einen optischen Empfänger, der einen optisch mit einer optischen Faser gekoppelten Fotodetektor (12) zum Empfangen von optischen Signalen über die Faser aufweist, der elektrisch mit der Eingangsstufe (10) verbunden ist, die Eingangsstufe (10) mit:

einem Puffer (14), der mit seinem Eingang mit dem Fotodetektor verbunden ist,
einem ersten Verstärker (16), der mit seinem Eingang mit dem Ausgang des Puffers (14) über eine erste Schaltvorrichtung (18) verbunden ist und eine erste zwischen den Ausgang des ersten Verstärkers (16) und den Eingang des Puffers (14) geschaltete hochwertige Rückkopplungswiderstandsvorrichtung (20) zum Definieren eines ersten Verstärkerkonfigurationsmodus für niedrige optische Signalpegel aufweist,
einem zweiten separaten Verstärker (24), der mit seinem Eingang mit dem Ausgang des Puffers (14) über eine zweite Schaltvorrichtung (22) verbunden ist und einen zweiten niederwertigen Rückkopplungswiderstand (26) aufweist, der zum Definieren eines zweiten Ver-

stärkerkonfigurationsmodus für große optische Signalpegel mit seiner einen Seite über eine dritte Schaltvorrichtung (28) mit dem Ausgang des zweiten separaten Verstärkers (24) und mit seiner anderen Seite mit dem Eingang des Puffers (14) verbunden ist, und
einer optischen Signalpegelerfassungs- und Schaltsteuervorrichtung (32, 34, 36), die mit dem Fotodetektor zum Erfassen des Pegels eines ankommenden optischen Signals und mit der ersten, der zweiten und der dritten Schaltvorrichtung zum Umschalten zwischen der ersten und der zweiten Verstärkerkonfiguration als Funktion des Signalpegels verbunden ist.

2. Transimpedanz-Eingangsstufe (10) nach Anspruch 1, wobei jeder Verstärker (16; 24) wenigstens zwei Verstärkertransistoren (Q2, Q5; Q3, Q4) aufweist.

3. Transimpedanz-Eingangsstufe (10) nach Anspruch 1 oder 2, wobei

der erste Verstärker (16) einen ersten Transistor (Q2) aufweist, der im Dualmodus

als die erste Schaltvorrichtung (18) zum selektiven Verbinden des ersten Verstärkers (16) mit dem Puffer (14) und
als ein Verstärkertransistor zum Verstärken eines Signals arbeitet, wenn die erste Verstärkerkonfiguration von der optischen Pegelerfassungs- und Schaltsteuervorrichtung (32, 34, 36) selektiert ist, und

der zweite Verstärker (24) einen zweiten Transistor (Q3) aufweist, der im Dualmodus

als die zweite Schaltvorrichtung (22) zum selektiven Verbinden des zweiten Verstärkers (24) mit dem Puffer (14) und
als ein Verstärkertransistor zum Verstärken eines Signals arbeitet, wenn die zweite Verstärkerkonfiguration von der optischen Pegelerfassungs- und Schaltsteuervorrichtung (32, 34, 36) selektiert ist.

4. Transimpedanz-Eingangsstufe (10) nach Anspruch 3, wobei jeder Verstärker (16; 24) einen separaten zusätzlichen Verstärkertransistor (Q5; Q4) aufweist.

5. Transimpedanz-Eingangsstufe (10) nach Anspruch 3 oder 4, wobei jeder Verstärker (16; 24) einen Komparator (U1B; U1D) mit einem Ausgang aufweist, der mit dem jeweiligen Dualmodus-Transistor (Q2; Q3) des Verstärkers (16; 24) verbundenen ist, wobei ein Eingang des Komparators (U1B; U1D) mit der optischen Pegelerfassungs- und Schaltsteuervorrichtung (32, 34, 36) verbunden ist.

6. Transimpedanz-Eingangsstufe (10) nach einem der Ansprüche 1 bis 5, wobei die dritte Schaltvorrichtung (28) einen Schalttransistor (Q6) zum selektiven Umschalten der Verbindung zwischen dem niederwertigen Rückkopplungswiderstand (26) und dem zweiten Verstärker (24) zwischen einer im wesentlichen offenen Schaltkreis- und einer geschlossenen Schaltkreiskonfiguration aufweist.

7. Transimpedanz-Eingangsstufe (10) nach einem der Ansprüche 1 bis 6, wobei die optische Pegelerfassungs- und Schaltsteuervorrichtung (32, 34, 36) eine Vorrichtung zum Mitteln eines Wertes eines erfaßten optischen Signalpegels und eine Zeitkonstantenvorrichtung aufweist, die eine ausreichend große Zeitkonstante bereitstellt, um zitterndes Umschalten zwischen der ersten und der zweiten Pegel-Verstärkerkonfiguration zu vermeiden.

8. Transimpedanz-Eingangsstufe (10) nach Anspruch 1, wobei die hochwertige Rückkopplungswiderstandsvorrichtung (20) einen resistiven Rückkopplungspfad definiert, der keine Elemente eines von der niederwertige Rückkopplungswiderstandsvorrichtung (26) definierten resistiven Rückkopplungspfads aufweist.

9. Transimpedanz-Eingangsstufe nach Anspruch 1, ferner mit einem Eingangsknoten, wobei

der Fotodetektor (12) mit dem Eingangsknoten verbunden ist,
der Puffer (14) einen Puffertransistor (Q1) mit einer mit dem Eingangsknoten verbundenen Basiselektrode und einem Kollektorausgang aufweist,
die erste Schaltvorrichtung (18) einen ersten Schalttransistor (Q2) mit einem mit dem Kollektorausgang verbundenen Emitter-Kollektor-Signalpfad, und einen ersten Komparator (U1B) zum Steuern einer Basiselektrode des ersten Schalttransistors (Q2) in Übereinstimmung mit einem Schaltsteuersignal (38) aufweist, das von der optischen Signalerfassungs- und Schaltsteuervorrichtung (32, 34, 36) erzeugt wird,
der erste Verstärker (16) eine erste Transistorverstärkervorrichtung (Q5) mit einem mit dem Emitter-Kollektor-Signalpfad des ersten Schalttransistors (Q2) verbundenen Eingang und einem mit einem Ausgangspuffer (Q7) verbundenen Ausgang aufweist,
die erste hochwertige Rückkopplungswiderstandsvorrichtung (20; R2, R3) zwischen den Ausgang der ersten Transistorverstärkervorrichtung (Q5) und den Eingangsknoten ge-

schaltet ist,
die zweite Schaltvorrichtung (22) einen zweiten Schalttransistor (Q3) mit einem mit dem Kollektorausgang verbundenen Emitter-Kollektor-Signalpfad, und einen zweiten Komparator (U1D) zum Steuern einer Basiselektrode des zweiten Schalttransistors (Q3) in Übereinstimmung mit dem Schaltsteuersignal (38) aufweist,
der zweite Verstärker (24) eine zweite Transistorverstärkervorrichtung (Q4) mit einem mit dem Emitter-Kollektor-Signalpfad des zweiten Schalttransistors (Q3) verbundenen Eingang und einem mit dem Ausgangspuffer (Q7) verbundenen Ausgang aufweist, und
die zweite niederwertige Rückkopplungswiderstandsvorrichtung (26) von dem Ausgang der zweiten Transistorverstärkervorrichtung (Q4) über die dritte Schaltvorrichtung (28) an den Eingangsknoten angeschlossen ist, wobei die dritte Schaltvorrichtung (28) einen dritten Schalttransistor (Q6) und einen dritten Komparator (U1C) zum Steuern einer Basiselektrode des dritten Schalttransistors (Q6) in Übereinstimmung mit dem Schaltsteuersignal (38) aufweist.

**Revendications**

1. Etage d'entrée (10) à adaptation d'impédance destiné à un récepteur optique comprenant un photodétecteur (12) couplé optiquement à une fibre optique pour la réception de signaux optiques par la fibre et raccordé électriquement à l'étage d'entrée (10), l'étage d'entrée (10) comprenant :

   un circuit tampon (14) raccordé par son entrée au photodétecteur,
   un premier amplificateur (16) raccordé par son entrée à la sortie du circuit tampon (14) par un premier dispositif (18) de commutation et comportant un premier dispositif (20) à résistance de réaction de valeur élevée connecté entre la sortie du premier amplificateur (16) et l'entrée du circuit tampon (14) pour la délimitation d'une configuration d'amplificateur à faible niveau des signaux optiques dans un premier mode,
   un second amplificateur séparé (24) connecté par son entrée à la sortie du circuit tampon (14) par un second dispositif de commutation (22) et possédant une seconde résistance de réaction de faible valeur (26) connectée par son premier côté, par l'intermédiaire d'un troisième dispositif de commutation (28), à la sortie du second amplificateur séparé (24) et, par son autre côté, à l'entrée du circuit tampon (14) pour la délimitation d'une configuration d'amplificateur à niveau élevé des signaux optiques dans un second mode, et
   un dispositif de commande de commutation et de détection de niveau optique (32, 34, 36) connecté au photodétecteur pour la détection d'un niveau de signal optique reçu et aux premier, second et troisième dispositifs de commutation entre la première et la seconde configuration d'amplificateur en fonction de celles-ci.

2. Etage d'entrée (10) à adaptation d'impédance selon la revendication 1, dans lequel chaque amplificateur (16 ; 24) comporte au moins deux transistors d'amplification (Q2, Q5 ; Q3, Q4).

3. Etage d'entrée (10) à adaptation d'impédance selon la revendication 1 ou 2, dans lequel le premier amplificateur (16) possède un premier transistor (Q2) qui travaille en mode double comme premier dispositif (18) de commutation pour la connexion sélective du premier amplificateur (16) au circuit tampon (14) et comme transistor d'amplification pour l'amplification d'un signal lorsque la première configuration d'amplificateur est sélectionnée par le dispositif (32, 34, 36) de commande de commutation et de détection de niveau optique, le second amplificateur (24) comportant un second transistor (Q3) qui travaille en mode double comme second dispositif de commutation (22) pour la connexion sélective du second amplificateur (24) au circuit tampon (14) et comme transistor d'amplification destiné à amplifier un signal lorsque la seconde configuration d'amplification est sélectionnée par le dispositif (32, 34, 36) de commande de commutation et de détection de niveau optique.

4. Etage d'entrée (10) à adaptation d'impédance selon la revendication 3, dans lequel chaque amplificateur (16 ; 24) possède un transistor d'amplification (Q5 ; Q4) supplémentaire séparé.

5. Etage d'entrée (10) à adaptation d'impédance selon la revendication 3 ou 4, dans lequel chaque amplificateur (16 ; 24) possède un comparateur (U1B ; U1D) ayant une sortie couplée à son transistor respectif à mode double (Q2 ; Q3), une entrée du comparateur (U1B ; U1D) étant connectée au dispositif (32, 34, 36) de commande de commutation et de détection de niveau optique.

6. Etage d'entrée (10) à adaptation d'impédance selon l'une quelconque des revendications 1 à 5, dans lequel le troisième dispositif de commutation (28) possède un transistor (Q6) de commutation sélective de la connexion entre la résistance de réaction de faible valeur (26) et le second amplificateur (24) essentiellement entre des configurations de circuit ouvert et de circuit fermé.

7. Etage d'entrée (10) à adaptation d'impédance selon l'une quelconque des revendications 1 à 6, dans lequel le dispositif (32, 34, 36) de commande de commutation et de détection de niveau optique comporte un dispositif destiné à former une moyenne d'une valeur d'un niveau de signal optique détecté et comporte un dispositif à constante de temps qui crée une constante de temps suffisamment longue pour empêcher une commutation par oscillation entre les configurations du premier et du second amplificateur de niveau.

8. Etage d'entrée (10) à adaptation d'impédance selon la revendication 1, dans lequel le dispositif à résistance de réaction de valeur élevée (20) délimite un trajet résistif de réaction qui ne comporte aucune partie d'un trajet résistif de réaction défini par le dispositif à résistance de réaction de faible valeur (26).

9. Etage d'entrée (10) à adaptation d'impédance selon la revendication 1, comprenant en outre un noeud d'entrée, dans lequel :

le photodétecteur (12) est connecté au noeud d'entrée,
le circuit tampon (14) comporte un transistor tampon (Q1) ayant une électrode de base connectée au noeud d'entrée et une sortie de collecteur,
un premier dispositif (18) de commutation comprenant un premier transistor de commutation (Q2) ayant un trajet de signal émetteur-collecteur connecté à la sortie de collecteur, et un premier comparateur (U1B) destiné à commander une électrode de base du premier transistor de commutation (Q2) en fonction d'un signal de commande de commutation (38) produit par le dispositif de commande de détection et de commutation (32, 34, 36) de niveau optique,
le premier amplificateur (16) comporte un premier dispositif amplificateur à transistor (Q5) ayant une entrée connectée au trajet de signaux émetteur-collecteur du premier transistor de commutation (Q2) et ayant une sortie connectée à un circuit tampon de sortie (Q7),
le premier dispositif à résistance de réaction de valeur élevée (20 ; R2, R3) est connecté entre la sortie du premier dispositif amplificateur à transistor (Q5) et le noeud d'entrée,
le second dispositif de commutation (22) possède un second transistor de commutation (Q3) ayant un trajet de signaux émetteur-collecteur connecté à la sortie de collecteur, et un second comparateur (U1D) destiné à commander une électrode de base du second transistor de commutation (Q3) en fonction du signal (38) de commande de commutation,
le second amplificateur (24) comporte un second dispositif amplificateur à transistor (Q4) ayant une entrée connectée au trajet des signaux émetteur-collecteur du second transistor de commutation (Q3) et ayant une sortie connectée au circuit tampon de sortie (Q7), et
le second dispositif à résistance de réaction de faible valeur (26) est connecté entre la sortie du second dispositif amplificateur à transistor (Q4), par l'intermédiaire du troisième dispositif à commutation (28), et le noeud de sortie, et le troisième dispositif de commutation (28) comporte un troisième transistor de commutation (Q6) et un troisième comparateur (U1C) destiné à commander une électrode de base du troisième transistor de commutation (Q6) en fonction du signal de commande de commutation (38).

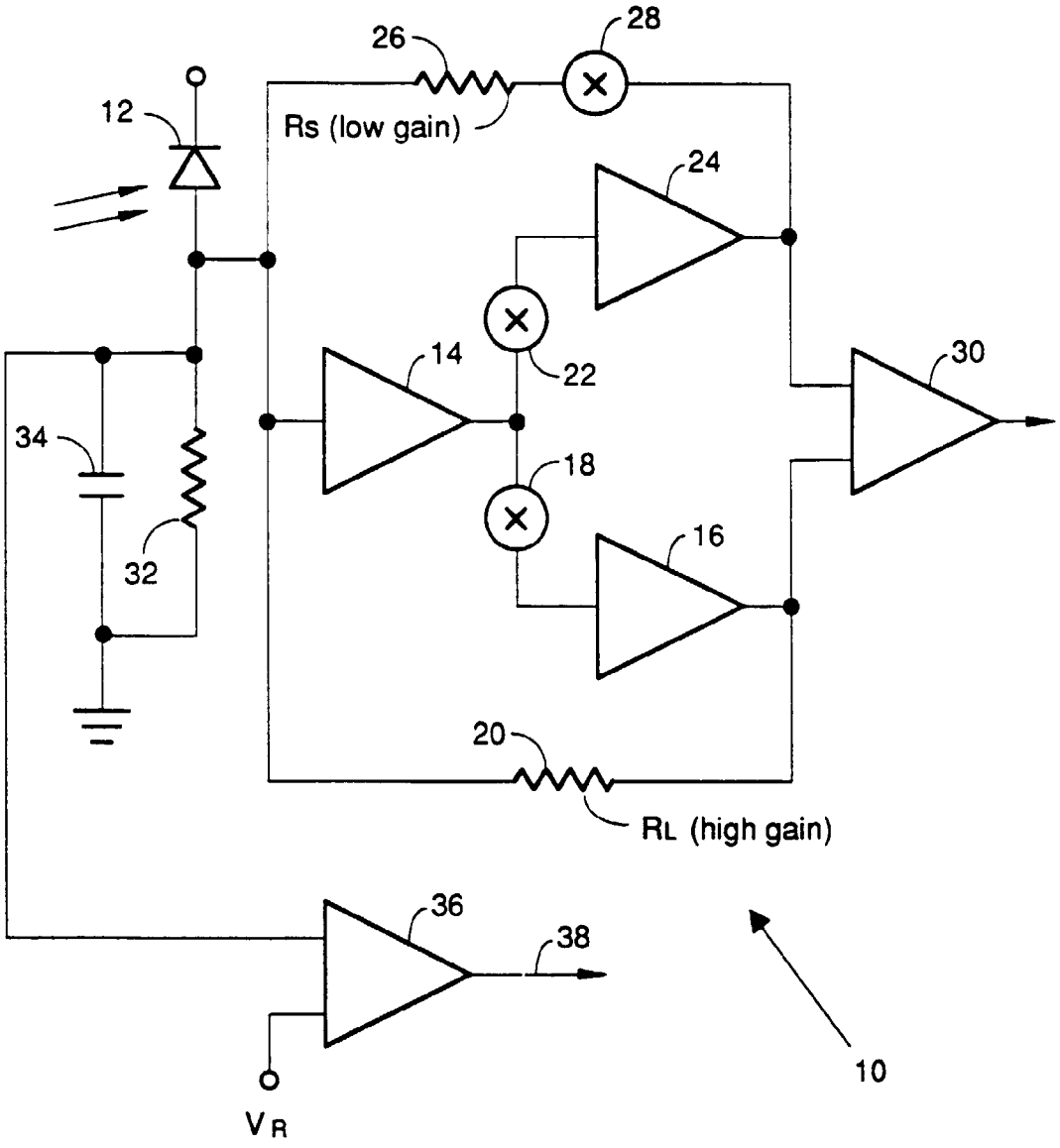
26
28
12
Rs (low gain)
24
14
22
30
34
18
16
32
20
RL (high gain)
36
38
10
VR

Fig 4

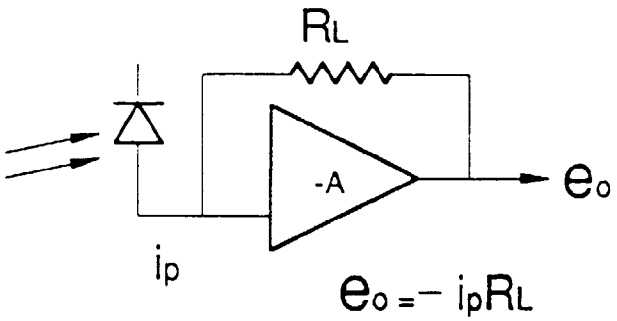


Fig 1 (Prior Art)

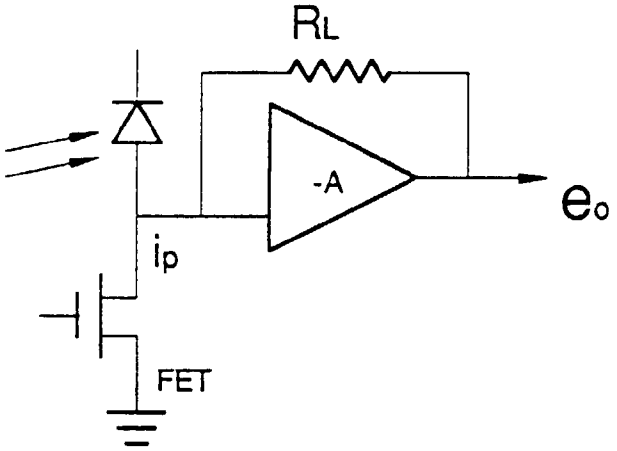


Fig 2 (Prior Art)

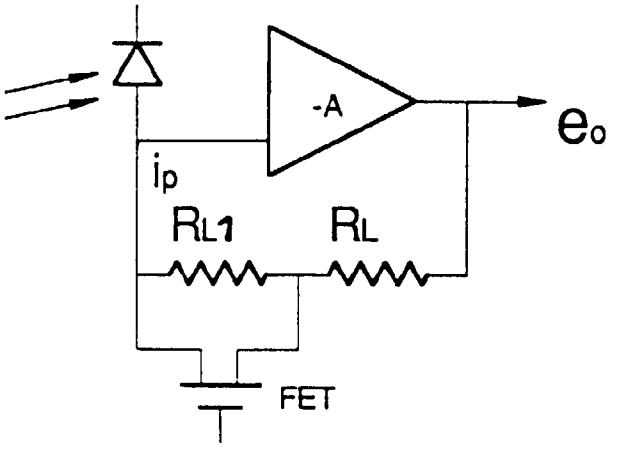


Fig 3 (Prior Art)

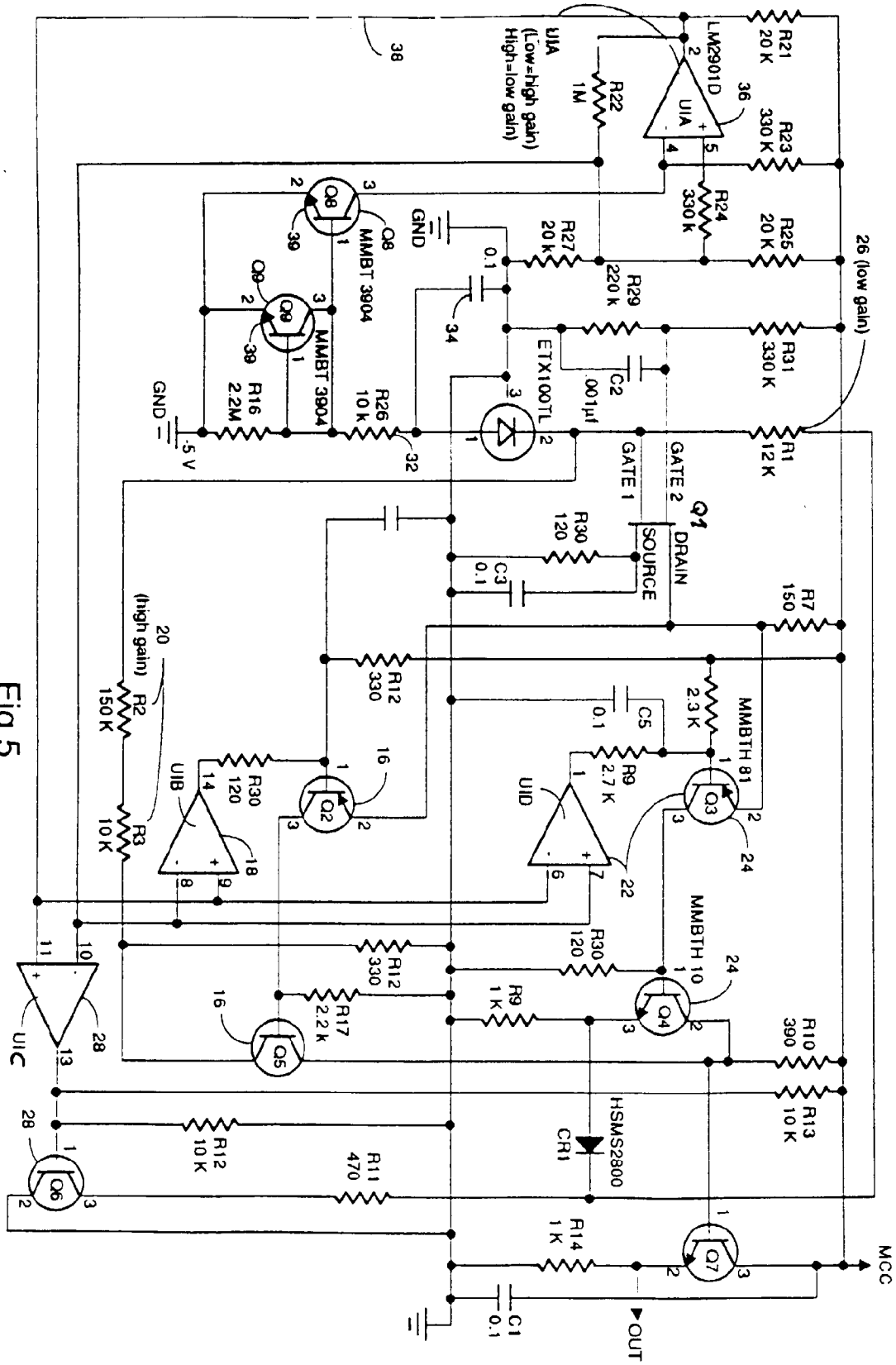
UIA
(Low=high gain)
High=low gain)
LM2901D
R21
20 K
R22
1M
R23
330 K
R24
330 k
R25
20 K
26 (low gain)
R27
20 k
R29
220 k
R31
330 K
R1
12 K
ETX100TL
C2
.001µf
GATE 1
GATE 2
Q1
SOURCE
DRAIN
R30
120
C3
0.1
R7
150
MMBTH 81
R12
330
C5
0.1
2.3 K
R9
2.7 K
UIB
UID
R2
150 K
(high gain)
R3
10 K
MMBTH 10
R17
2.2 k
R10
390
R13
10 K
HSMS2800
CR1
R12
10 K
R11
470
R14
1 K
C1
0.1
MCC
OUT
GND
-5 V
MMBT 3904
R16
2.2M
R26
10 k
UIC
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9

Fig 5